REMARKS

Claims 1-10 and 12-35 are pending. Claims 1, 12, 16, 24, 30, and 33 are independent and claims 22-35 are newly added. In the Office Action, claims 1-8 and 16-19 were rejected under 35 U.S.C. §102(b) as being anticipated by Panchul et al. (USPN 6,226,776). Claim 9 was rejected under 35 U.S.C. §103(a) as being unpatentable over Panchul et al. in view of Davis et al. (USPN 6,230,307). Claim 10 was rejected under 35 U.S.C. §103(a) as being unpatentable over Panchul et al. in view of Kodosky et al. (USPN 6,584,601). Claims 12-14 and 20-21 were rejected under 35 U.S.C. §103(a) as being unpatentable over Panchul et al. in view of Kim et al. (USPN 6,513,144). These rejections are respectfully traversed.

ALLOWABLE SUBJECT MATTER

The Office Action states claims 11 and 15 include allowable subject matter and would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims. Claim 1 has been amended to include all the features of claim 11, and thus claims 1-10 are believed to be allowable.

REJECTIONS UNDER 35 U.S.C. § 102(b)

Claims 1-8 and 16-19 were rejected under 35 U.S.C. §102(b) as being anticipated by Panchul et al. The Office Action states claim 11 includes allowable subject matter and would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims. Claim 1 has been amended to include all the features of claim 11, and thus claims 1-8 are believed to be allowable. Independent claim 16 has been amended to include the features of claim 11, and thus claims 16-19 are believed to be allowable.

REJECTIONS UNDER 35 U.S.C. § 103(a)

Claim 9 was rejected under 35 U.S.C. §103(a) as being unpatentable over Panchul et al. in view of Davis et al. Claim 10 was rejected under 35 U.S.C. §103(a) as being unpatentable over Panchul et al. in view of Kodosky et al. Claims 9 and 10 are dependent on claim 1, and claims 9 and 10 are believed to be allowable for at least the same reasons as claim 1 is believed to be allowable.

Claims 12-14 and 20-21 were rejected under 35 U.S.C. §103(a) as being unpatentable over Panchul et al. in view of Kim et al. The rejection of claim 12 correctly states that Panchul et al. does not disclose identifying a set of assumable values for each of the identified variables and calculating a set of assumable values for other variables holding the results of the operation based on the identified set of assumable values. The rejection, however, combines Kim et al. with Panchul et al., stating Kim et al. discloses these steps in column 3, lines 50-52 and column 11, lines 19-23.

Kim et al. discloses a method for generating test data for testing a simulated circuit design. A hardware verification language (HVL) is used to test a circuit design. Kim et al. discloses using the HVL to generate random value test data for testing a circuit design. *See* column 2, lines 6-16 and column 5, lines 24-27.

Claim 12 has been amended to recite, "receiving user code, wherein the user code is an expression of a design of a digital circuit." Claim 12 also recites, "calculating a set of assumable values for other variables in the user code holding the results of the operation based on the identified set of assumable values."

Kim et al. fails to teach or suggest user code that is an expression of a design of a digital circuit. Kim et al. also fails to teach or suggest calculating a set of assumable values for other variables in the user code holding the results of the operation. Instead, the HVL code in Kim et al. is used to generate random values for testing a design of a circuit, rather

than being an expression of the actual design of the circuit. Specifically, Kim et al. discloses using tuples in HVL code to express a range of random values a variable may assume for test data. The range of values is for a variable used in HVL code and not in user code that is an expression of a design of a digital circuit.

In addition, the tuples of Kim et al. are not based on an identified set of assumable values for variables used in the operation. A tuple in Kim et al., shown in figure 6 of Kim et al., provides a format for expressing in a VRL computer program a range of random values for a variable (*e.g.*, the variable X). The tuples are not based on other variables in the VRL computer program, such as a variable Y that may also be used in the same VRL computer program. Thus, Kim et al. fails to teach or suggest calculating a set of assumable values for a variable holding the results of an operation using another variable. Accordingly, the combination of Panchul et al. in view of Kim et al. fails to teach or suggest each and every feature of claim 12.

Furthermore, it would not have been obvious to one of ordinary skill in the art to combine Kim et al. with Panchul et al., because Kim et al. is directed to generating random values for test data used to test a circuit design, and Panchul et al. is directed to configuring an FPGA rather than generating test data for testing a configuration of an FPGA. In addition, the rejection states it would have been obvious to combine Kim et al. with Panchul et al. because,

> Calculating a set of assumable variables as discloses by Kim would have improved Panchul's system by providing defined ranges for variables in Panchul's algorithm specification which would give a designed control over the design parameters and specifications of the circuit representation.

The proposed combination of Kim et al. with Panchul et al. results in using the tuples of Kim et al., which are used to define a range of random values a variable may assume, to configure an FPGA. It is unclear how limiting a range of random values that a variable may assume can be used to configure an FPGA in Panchul et al., let alone improve a designer's control over the configuration of an FPGA. On the contrary, using random values to configure an FPGA is likely to result in a designer having less control over the configuration of an FPGA, because the designer has less control over the value selected for the variable affecting the configuration of the FPGA. For at least these reasons claims 12-14 are believed to be allowable.

Claims 20-21 are dependent on claim 16 and are believed to be allowable for at least the same reasons claim 16 is believed to be allowable. In addition claims 20-21 recite features similar to claim 12 and are believed to be allowable for the same reasons claim 12 is believed to be allowable.

NEWLY ADDED CLAIMS

Claims 22-35 are newly added of which claims 24, 30, and 33 are independent. Claims 22 and 23 are dependent on claim 12 and are believed to be allowable for at least the same reasons claim 12 is believed to be allowable.

Claim 24 includes receiving high level programming language code representing an expression of a design of a digital circuit, wherein the code comprises at least one algorithm specification, at least one data representation specification, and at least one data communication specification identifying a data communication implementation in the digital circuit. Panchul et al. fails to teach or suggest at least one data communication specification identifying a data communication implementation in the digital circuit. The rejection of

claim 9 combines the teachings of Davis et al. with Panchul et al. to teach a data communication specification. Specifically, the rejection of claim 9 states that Davis et al. discloses a data communication specification in column 13, lines 16-23.

Davis et al. discloses a system for configuring FPGAs. In column 13, lines 16-23, Davis et al. discloses that different FPGAs may use different interfaces, such as a 32-bit memory interface and a 1-bit serial interface. Davis et al. discloses an abstraction layer that transparently maps high level functions into low level operations on the FPGA hardware using a particular interface. Thus, a designer need not know or specify information about the FPGA control interface when providing instructions for configuring the FPGA. Accordingly, Davis et al. fails to teach or suggest providing code for configuring a circuit that includes a data communication implementation. Instead, in Davis et al., a particular interface for an FPGA is transparently determined by an abstraction layer rather than being designated in high level programming language code, for example, provided by a designer. Accordingly, claims 24-29 are believed to be allowable.

Independent claims 30 and 33 include features similar to claim 1, and thus claims 30-35 are believed to be allowable for at least the same reasons claim 1 is allowable.

CONCLUSION

As all of the outstanding rejections have been traversed and all of the claims are believed to be in condition for allowance, the Applicant respectfully requests issuance of a Notice of Allowability. If the undersigned attorney can assist in any matters regarding examination of this application, the Examiner is encouraged to call at the number listed below.

Respectfully submitted,

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By _____

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